SCHS309B - JANUARY 2001 - REVISED MAY 2002

 Inputs Are TTL-Voltage Compatible Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption 	CD54ACT02 F PACKAGE CD74ACT02 E OR M PACKAGE (TOP VIEW)
Balanced Propagation Delays	
 ±24-mA Output Drive Current – Fanout to 15 F Devices 	1A [] _{2 13}] 4Y 1B [] 3 12] 4B
 SCR-Latchup-Resistant CMOS Process and Circuit Design 	2Y [] 4 11 [] 4A 2A [] 5 10 [] 3Y
 Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015 	2B [6 9] 3B GND [7 8] 3A

description

The 'ACT02 devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – E	Tube	CD74ACT02E	CD74ACT02E
55°C to 125°C	°C to 125°C SOIC – M	Tube	CD74ACT02M	ACT02M
–55°C to 125°C		Tape and reel	CD74ACT02M96	ACTOZINI
	CDIP – F	Tube	CD54ACT02F3A	CD54ACT02F3A

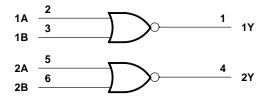
ORDERING INFORMATION

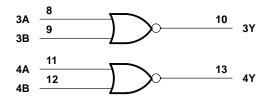
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

(each gate)						
INP	UTS	OUTPUT				
Α	В	Y				
Н	Х	L				
Х	н	L				
L	L	н				

logic diagram (positive logic)







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SCHS309B - JANUARY 2001 - REVISED MAY 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 6 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) (see Note 1)	
Output clamp current, I_{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	80°C/W
M package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		T _A = 25°C		–40°C TO 85°C		–55°C TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
VIL	Low-level input voltage		0.8		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	0	VCC	V
VO	Output voltage	0	VCC	0	VCC	0	VCC	V
ЮН	High-level output current		-24		-24		-24	mA
IOL	Low-level output current		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	TEST CONDITIONS	Vcc	V _{CC} T _A = 25°C		–40°C TO 85°C		–55°C TO 125°C		UNIT
				MIN	MIN MAX MIN		MAX	MIN	MAX	
		I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4		
Vau	$\lambda = \lambda + \sigma \lambda + \sigma$	I _{OH} = -24 mA	4.5 V	3.94		3.8		3.7		V
Vон	$V_{I} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \text{ mA}^{\ddagger}$	5.5 V					3.85		v
		$I_{OH} = -75 \text{ mA}^{\ddagger}$	5.5 V			3.85				
		l _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	
Val	$V_I = V_{IH} \text{ or } V_{IL}$	I _{OL} = 24 mA	4.5 V		0.36		0.44		0.5	V
VOL		I _{OL} = 50 mA‡	5.5 V						1.65	v
		I _{OL} = 75 mA‡	5.5 V				1.65			
lj	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
ICC	$V_I = V_{CC}$ or GND,	I <mark>O</mark> = 0	5.5 V		4		40		80	μΑ
ΔICC	$V_{I} = V_{CC} - 2.1 V$		4.5 V to 5.5 V		2.4		2.8		3	mA
Ci					10		10		10	pF

[‡] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



SCHS309B - JANUARY 2001 - REVISED MAY 2002

ACT INPUT LOAD TABLE

INPUT UNIT LOAD A or B 0.32 Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

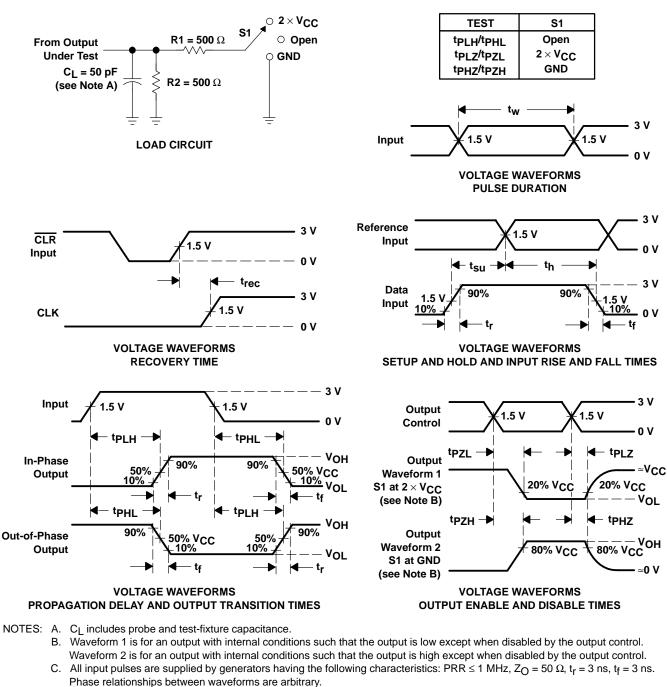
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°0 85°		–55°C 125		UNIT
(INPOT)		MIN	MAX	MIN	MAX		
^t PLH	A or B	Y	3.1	11.1	3.1	12.2	
^t PHL	AUB	I	3.1	11.1	3.1	12.2	ns

operating characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	55	pF

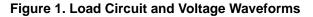


SCHS309B – JANUARY 2001 – REVISED MAY 2002



PARAMETER MEASUREMENT INFORMATION

- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. tPLZ and tPHZ are the same as tdis.





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